# e2V

# CCD42-40 Front Illuminated NIMO Ceramic Compact Pack Large Area Sensor for Scientific Applications

# e2v technologies

#### **FEATURES**

- 2048 x 2048 x 13.5 μm pixels
- Front Illuminated Operation
- Low Noise Output Amplifier
- Dual Responsivity Output
- Full-frame Architecture
- Gated Dump Drain on Output Register
- Compact Footprint Ceramic Package

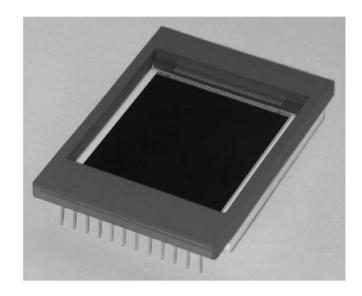
#### INTRODUCTION

This version of the CCD42 family of CCD Sensors has full-frame architecture, which in combination with an extremely low noise amplifier, makes the device well suited for use in general scientific imaging.

The output amplifier is designed to give excellent noise levels at low pixel rates and can match the noise performance of most conventional science CCDs at pixel rates as high as 3 MHz.

There are two low noise amplifiers in the readout register, one at each end. Charge can be made to transfer through either or both amplifiers by making the appropriate RØ connections. The readout register has a gate controlled dump drain to allow fast dumping of unwanted data.

The register is designed to accommodate four image pixels of charge and a summing well is provided, capable of holding six image pixels of charge. The output amplifier has a feature (switchable OG2) to enable the responsivity to be reduced, allowing the reading of such large charge packets.



#### **GENERAL DATA**

#### **Format**

Image area Active pixels:											27.6 x 27.6 mm
											2048
											2048 + 4
serial overse	car	ηр	ixel	ls							50 at each end
Pixel size .											13.5 x 13.5 μm
Number of ou	ıtpı	ut	am	plif	iers	6					2
The device has a 100% fill factor for maximum sensitivity.											
Spectral range	е										. 420 - 1060 nm

### **PERFORMANCE LIMITS**

	Min	Typical	Max	
Peak charge storage (see note 1)	100k	150k	-	e <sup>-</sup> /pixel
Peak output voltage (unbinned)	-	675	-	mV
Dark signal at 293 K (see note 2)	-	10,000	25,000	e <sup>-</sup> /pixel/s
Dark signal at 243 K (see note 2)	-	63	-	e <sup>-</sup> /pixel/s
Charge transfer efficiency (see note 3): parallel serial	99.999 99.999	99.9999 99.9993	-	% %
Output amplifier responsivity: normal mode high signal mode	3.0	4.5 1.5	6.0	μV/e <sup>-</sup> μV/e <sup>-</sup>
Readout noise at 243 K (see note 4)	-	3.0	4.0	rms e <sup>-</sup>
Readout frequency (see note 5)	-	20	3000	kHz
Line transfer period	10	20	-	μs
Output node capacity (see note 6)	-	1,000,000	-	e <sup>-</sup>

#### **NOTES**

- 1. Signal level at which resolution begins to degrade.
- 2. The typical average (background) dark signal at any temperature T (kelvin) between 230 K and 300 K is given by:

$$Q_d/Q_{do} = 122T^3e^{-6400/T}$$

where Q<sub>do</sub> is the dark current at 293 K. Note that this is typical performance and some variation between devices may be seen.

- 3. CTE is measured for a complete 3-phase clock triplet.
- 4. Measured using correlated double sampling. Noise specification applies at 20 kHz.
- 5. Readout above 3000 kHz can be achieved but performance to the parameters given cannot be guaranteed.
- 6. With output circuit configured in low responsivity/high capacity mode (OG2 high).

#### TYPICAL OPERATING CONDITIONS

Ref	Pin No.	Typical Voltage
SS	1, 12, 13, 24	9.5 V
IØ1	17	12 V
IØ2	18	12 V
IØ3	16	12 V
RØ1(L)	20	11 V
RØ2(L)	19	11 V
RØ1(R)	22	11 V
RØ2(R)	23	11 V
RØ3	21	11 V
ØR	14	12 V
ØSW	15	11 V
DG (see note 9)	7	0 V
OG1	2	3 V
DD	6	24 V
OG2	11	see note 7
OD(L)	4	29 V
OD(R)	9	29 V
OS(L)	3	see note 8
OS(R)	10	see note 8
RD(L)	5	17 V
RD(R)	8	17 V

#### Nomenclature

									Substrate trate (connect to SS)
									Image area clocks
									Serial register clocks
ØR									Reset clock
ØS'	W								. Summing well
DG									Register dump gate
OG1	, C	)G2	-						Output gates
DD									Dump drain
OD									Output drain
OS									. Output source
RD									Reset drain

#### **NOTES**

- 7. OG2 = OG1 + 1 V normal low noise mode or OG2 = 20 V low responsivity/increased charge handling mode.
- 8. OS = 3 to 5 V below OD typically. Use 3 5 mA current source or 5 10 kW load.
- 9. Non-charge dumping level is shown. For charge dumping, DG should be pulsed to 12  $\pm$  2 V.
- 10. Readout register clock pulse low levels +1 V; other clock low levels 0  $\pm$  0.5 V.
- 11. With the RØ connections shown, this device will operate through both outputs. In order to operate from the left-hand output only, RØ1(R) and RØ2(R) should be reversed.

#### **BLEMISH SPECIFICATION**

Traps	Pixels where charge is temporarily held.
	Traps are counted if they have a capacity
	greater than 200 $e^-$ at 243 K.

Black spots Are counted when they have a signal level of less than 90% of the local mean at a

of less than 90% of the local mean at a signal level of approximately half full-well.

White spots

Are counted when they have a generation

rate 125 times the specified maximum dark signal generation rate (measured between 243 and 293 K). The typical temperature dependence of white spot defects is the same as that of the average dark signal, i.e.:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

**Column defects** A column that contains at least 21 white or 21 black defects.

GRADE	0	1	2
Column defects	0	1	4
Black spots	50	75	100
Traps > 200 e <sup>-</sup>	10	20	30
White spots	50	75	100

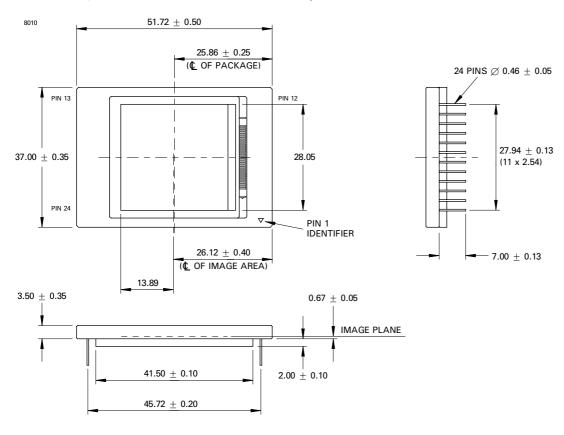
**Grade 5** Functional devices for set-up purposes only.

## Part Reference

CCD42-40-\*-382 \*= grade, non-IMO, frontside, ceramic compact package.

Other variants of the CCD42-40 available are back illuminated format and advanced inverted mode operation (AIMO). In common with all e2v technologies CCD Sensors, the front illuminated CCD42-40 is available with a fibre-optic window or taper, or with a phosphor coating. Sensors are normally supplied with a temporary glass window. The CCD42-40 is also available in a PGA metal pack or on a metal 3-side buttable package.

## **OUTLINE** (All dimensions in millimetres; dimensions without limits are nominal)



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